REMARKS

Reconsideration of this application in its continued examination, based on this amendment and these following remarks, is respectfully requested.

Claims 1, 3, 5, 10, 15, 19, 22, 49, and 50 remain in this case. Claims 1, 3, 5, 10, 19, 22, 49, and 50 are amended. Claims 4 and 43 through 48 are newly canceled.

Claims 1, 3 through 5, 10, 15, 19, 22, and 43 through 50 were previously finally rejected under §112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner found that independent claims 1 and 22 as amended in the previous response are not supported by the specification of this application.

While claims 1 and 22 are amended in this paper, the limitations in previously presented claims 1 and 22 that the Examiner found to not be supported, in making the §112 rejection, remain in the claims. Applicants therefore hope to more thoroughly explain the manner in which the specification of this application supports previously amended independent claims 1 and 22.

In this regard, Applicants will illustrate this support of each element of amended claim 1 by way of an explicit example that is present in the specification[1]. This illustration of support is not intended to limit the scope of claim 1 in any way, and as such it is to be understood that the scope of claim 1 is not intended to be limited to this example from the specification. Rather, this illustration is intended merely to clarify the support in the specification for the limitations of independent claim 1, as amended in this response.

Claim 1	Example in the specification
A method for performing a write operation in a non-volatile memory system, the non-volatile memory system including an MLC NAND flash non-volatile memory having a plurality of erase units, each erase unit including a plurality	The Office Action raises no issue regarding support for the preamble. By way of example, the "erase unit" of the claim corresponds to physical block **300**, and

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[1] *See* specification of S.N. 10/679,008, *as published as* U.S. Patent Application Publication No. US 2004/0103241 A1, paragraphs [0046] through [0050].

of programming units arranged in a sequence, each programming unit comprising a plurality of non-volatile memory cells, wherein a first logical block is mappable to one or more erase units and includes a plurality of logical pages arranged in a sequence, the method comprising:	the "programming units" of the claim correspond to pages **304.**[2] The "logical sub-units" of the claim correspond to pages of the logical block that is mapped to physical block **300**; these pages of the logical block are disclosed as being in a sequence.[3]
writing data associated with the first logical block into an original erase unit to which the first logical block is mapped, so that data associated with the logical pages are written into corresponding programming units in that original erase unit in sequence;	The "original erase unit" containing data associated with a first logical block corresponds to "original" physical block **400**.[4]
grouping the programming units within a first update erase unit into a plurality of groups of programming units, the programming units within each group arranged in a sequence comprising a first programming unit, a second programming unit, and a third programming unit;	Pages **304** within physical block **300** are grouped into a plurality of groups **308**.[5] The pages **304** within each group **308** are arranged in sequence.[6] For example, pages **304a, 304b, 304c, 304d** are in sequence in first group **308a.** Pages **304e** through **304h** are in sequence in second group **308b.** In this example: the first programming unit in group **308a** is page **304a**; the second programming unit in group **308a** is page **304c**, and the second programming unit in group **308b** is page **304g**; and the third programming unit in group **308a** is page **304d**.
writing contents of an updated first logical page into the first programming unit in a first group of programming units of the first update	Contents **312** of the first page of the logical block are written into page **304a** of group **308a** of block **300**. Updated contents **430** are

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[2] Specification, *supra,* paragraph [0044]; Figure 3.

[3] Specification, *supra,* paragraphs [0045]. Paragraph [0051] also discloses the sequence of logical pages, in the alternative approach in which the logical pages are also grouped into logical groups.

[4] Specification, *supra,* paragraphs [0058] and [0061]; Figure 4b.

[5] Specification, *supra,* paragraph [0044]; Figure 3.

[6] Specification, *supra,* paragraphs [0044] and [0045]; Figure 3. *See also* block **420** of Figure 4b.

erase unit;	written into page **424a** of group **428a** of block **420.**[7]
writing contents of an updated third logical subpage into the third programming unit of the first group of programming units, the third logical page later in the sequence of logical pages than the first logical page, and the third programming unit later in the sequence of programming units within the first group than the first programming unit and the second programming unit;	Contents **314** of the fourth page of the logical block are stored in page **304d** of group **308a** of block **300**.[8] These contents **314** are written to page **304d** after contents **312** are written into page **304a** because "[p]ages **304** within a group **308** may generally only be written sequentially such that no lower or previous page **304** may be written to once a higher page **304** has been written to."[9] Contents **434** from the eighth logical page **404b** are written into the eighth physical page **424c** of group **428a**.[10]
receiving contents of an updated second logical page of the first logical block, the second logical page earlier in the sequence of logical pages than the third logical page;	Contents **316**; contents **436**.[11]
determining whether one of the groups of programming units in the first update erase unit is available for writing into;	Decision **508**.[12]
responsive to a group of programming units being available in the first update erase unit, writing the updated contents of the second logical page into a programming unit in an available group of programming units of the first update erase unit; and	Contents **316** are then written into page **304g** of group **308b**.[13] Contents **436** are then written into page **424e** of group **428b**.[14] Process **516**.[15]
responsive to a second group of programming units not being available in the first update	Decision **508**; processes **524, 528, 532**.[16]

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[7] Specification, *supra,* paragraph [0045] and [0053]; Figure 4b.
[8] Specification, *supra,* paragraph [0045].
[9] Specification, *supra,* paragraph [0046].
[10] Specification, *supra,* paragraph [0054].
[11] Specification, *supra,* paragraphs [0046] and [0055]
[12] Specification, *supra,* paragraph [0067]; Figure 5.
[13] Specification, *supra,* paragraph [0046].
[14] Specification, *supra,* paragraph [0055].
[15] Specification, *supra,* paragraph [0068]; Figure 5.
[16] Specification, *supra,* paragraphs [0070] and [0071]; Figure 5.

erase unit, merging contents associated with the first logical unit stored in the original erase unit and updated contents of the first logical block stored in the first update erase unit into a second update erase unit.	

It appears, from the Office Action,[17] that the Examiner considered contents **316** of the third page of the logical block to correspond to the third logical sub-unit of the claim, contents **312** of the first page of the logical block to correspond to the first page of the logical sub-unit of the claim, and contents **318** of the second page of the logical block to correspond to the second logical sub-unit of the claim. As indicated above, this correspondence is incorrect. For purposes of support of this claim, as noted above, contents **312** of the first page of the logical block correspond to the first page of the logical page of the claim, contents **316** of the fourth page of the logical block correspond to the *third* logical page of the claim, and contents **316** of the third page of the logical block correspond to the *second* logical page of the claim. Applicants submit that, if the specification is considered in this manner, its support of amended claim 1 will be evident.

In addition, the Examiner also asserted that the specification describes "the write operations in a general manner without any particular sequence by using the word 'when', as opposed to the word 'then'".[18] Applicants dispute this point. As noted above, the specification clearly and unambiguously states that "[p]ages **304** within a group **308** may generally only be written sequentially such that no lower or previous page **304** may be written to once a higher page **304** has been written to."[19] Because of this sequential-write restriction, within groups of pages of a physical block, one can readily deduce the *temporal* order in which pages within a group are written from the *physical* position of the page contents once written. Because of this sequential-write restriction, page **304d** of group **308a** in Figure 3 is necessarily written after page **304a** in that group **308a**. Furthermore, according to the example of the claimed invention described at this portion of the specification, this sequential-write restriction is the very reason that contents **316** are written into page **304g** of group **308b**, rather than into page **304c** of group

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[17] Office Action of January 18, 2008, page 3.
[18] Office Action, *supra,* page 3.
[19] Specification, *supra,* paragraph [0046].

308a – because page **304c** cannot be written after page **304d** has been written. This described operation is consistent with the recitation of the steps present in amended claim 1.

Claim 1 is also amended to clarify its patentability over the prior art, as will be discussed below, and for clarity. It is submitted that the new steps recited in claim 1 are also clearly supported by the specification, as indicated in the above claim chart and the cited locations thereat.

Independent apparatus claim 22, specifically the recited sequence of operations according to which the controlling means writes contents into the memory, as amended, is supported in the same manner as described above relative to claim 1.

Applicants therefore submit that amended independent claims 1 and 22 are clearly and fully supported by the written description in the specification of this application. Applicants request reconsideration of these claims.

Previously presented claims 1, 3 through 5, 10, 15, 19, 22, and 43 through 50 were finally rejected under §103 as unpatentable over the Miyauchi reference[20] in view of the Kramer reference.[21]

Claim 1 is amended to advance the prosecution of this case by further clarifying its distinction over the Miyauchi reference. Amended claim 1 now recites the step of writing data associated with the first logical block into an original erase unit, and that the grouping and writing steps recited in the claim are applied to a first update erase unit, into which updated contents of logical pages of the first logical block are written. Upon receiving contents of an updated second logical page that is earlier in the sequence of logical pages than the third logical page, the claimed method now requires determining whether a group of programming units in the first update erase unit is available for writing into; if not, the method requires merging contents associated with the first logical unit that are stored in the original erase unit, and updated contents stored in the first update erase unit, into a second update erase unit. No new matter is presented by this amendment to claim 1, given its clear support in the specification as discussed above.

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[20] U.S. Patent No. 6,430,650 B1, issued August 6, 2002 to Miyauchi, from an application filed June 17, 1996.

[21] U.S. Patent No. 6,182,239 B1, issued January 30, 2001 to Kramer.

Claims 3, 5, 10, and 49 are amended, and claims 4 and 43 through 45 are canceled, for consistency with the amendment to claim 1.

The method of amended claim 1 and its dependent claims provides important advantages over the prior art, including the Miyauchi and Kramer references of record in this case. In particular, the inventive method enables out-of-sequence write operations to be performed in an MLC NAND flash memory, in which out-of-sequence writes are otherwise prohibited, without consuming another erase unit, or physical block, to do so.[22] In addition, the method of amended claim 1 accomplishes these advantages in a manner that occupies only an original physical block and one update block, for a given logical block, following which the original data and updates are merged into a new physical block.[23] The claimed method thus improves the flexibility and performance of writing data in this important and widely-used type of flash memory, reduces erase wear, and efficiently maintains physical block usage in such devices.

Applicants submit that amended claim 1 and its dependent claims are novel and inventive over the Miyauchi and Kramer references, as well as the other prior art of record in this case.

Both the Miyauchi and Kramer references lack any teachings or suggestion regarding the merging or other management of data in various physical blocks, or erase units as recited in the claims. The teachings of the Miyauchi reference[24] that were asserted by the Examiner as teaching the "merge operation",[25] refer to the merging of data within physical groups PGN within a single physical block.[26] There is no mention whatsoever in the Miyauchi reference of any merging of data from multiple physical blocks, associated with a logical block, much less disclosure or suggestion of the operations now required of amended claim 1. The Kramer reference is also silent in this regard. Accordingly, Applicants submit that the combined teachings of the applied references fall short of the requirements of amended claim 1 and its dependent claims as now presented in this case.

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[22] Specification, *supra,* paragraphs [0009] through [0011], [0050], [0077].

[23] Specification, *supra,* paragraphs [0058] through [0071]; Figures 4b, 4c, and 5.

[24] Miyauchi, *supra,* column 7, lines 20 through 36; Figures 8A through 8E.

[25] Office Action, *supra,* page 20.

[26] Miyauchi, *supra,* column 4, lines 6 through 10 ("For example, if 60 groups exist in the erase block 20, 60 sets of group management information are stored."); column 7, lines 22 through 24 ("FIGS. 8A, 8B, 8C, 8D, and 8E show group management data for physical group number PGN of A, B, C, D, E.").

Furthermore, Applicants submit that one skilled in the art would not obviously arrive at the method of amended claim 1, given the teachings of the Miyauchi and Kramer references, or the other prior art of record in this case. Applicants therefore submit that amended claim 1 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

Claim 22 is similarly amended as claim 1, discussed above. Amended claim 22 now recites that the non-volatile memory includes means for mapping each of a plurality of logical blocks with corresponding erase units. Amended claim 22 now also recites that the means for controlling the writing of contents does so according to a sequence of operations that now further comprises writing data associated with the first logical block into an original erase unit, and that the grouping and writing operations are applied to a first update erase unit, into which updated contents of logical pages of the first logical block are written. The sequence of operations now also requires receiving contents of an updated second logical page that is earlier in the sequence of logical pages than the third logical page, determining whether a group of programming units in the first update erase unit is available for writing into, and if not, merging contents associated with the first logical unit that are stored in the original erase unit, and updated contents stored in the first update erase unit, into a second update erase unit. This amendment to claim 22 is supported in the same manner as discussed above relative to amended claim 1, and as such no new matter is presented.

Claims 19 and 50 are amended, and claims 46 through 48 are canceled, for consistency with the amendment to claim 22.

The system of amended claim 22 and its dependent claims provides similar advantages over the prior art as does the method of amended claim 1, discussed above. In short, these advantages include the ability to perform out-of-sequence write operations in an MLC NAND flash memory in which out-of-sequence writes are otherwise prohibited, while reducing erase wear, and improving the efficiency of physical block usage in the non-volatile memory.

For similar reasons as discussed above, Applicants submit that neither of the Miyauchi and Kramer references disclose or suggest the merging of erase units in a non-volatile memory whatsoever, much less in the manner now recited as carried out by the controlling means of amended claim 22. Furthermore, Applicants submit that a person of ordinary skill in the art would not be motivated to modify these combined teachings of the Miyauchi and Kramer references, nor would that person use his or her ordinary creativity to so modify these teachings, in such a manner as to reach amended claim 22.

Applicants therefore submit that amended claim 22 and its remaining dependent claims are novel and patentably distinct over the prior art of record in this case.

For these reasons, Applicants respectfully submit that the claims now in this case are in condition for allowance. Favorable reconsideration of this application in light of this amendment, upon its continued examination, is respectfully requested.

Respectfully submitted,

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